What is claimed is:

1. A variable length coding unit comprising:

a run-length converter for converting block data consisting of a plurality of image signals into combined data in accordance with a scanning sequence, each of the combined data including a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients;

a table memory for storing a variable length code and its code length corresponding to the combined data at an address corresponding to the combined data; and

variable length encoder for reading the variable length code and its code length from said table memory in accordance with the combined data converted by said run-length converter, and for carrying out variable length coding of the variable length code by cutting it from the read data in accordance with the code length.

2. The variable length coding unit according to claim 1, further comprising:

a buffer memory for recording variable length coded data passing through the variable length coding by said variable length encoder;

a shifter for shifting the variable length coded data by a predetermined number of bits, when the variable length coded data stored in said buffer memory exceeds the predetermined number of bits;

a data output section for outputting the variable length coded data undergoing the bit shift by the predetermined number of bits by said shifter; and

a processor for activating and controlling at least part of said run-length converter, said variable length encoder, said buffer memory, said shifter and said data output section.

3. The variable length coding unit according to claim 2, wherein said table memory has a word width of L bits, and stores the variable length code with a maximum length of m bits from a most significant bit side of the L-bit width, and its code length with a length of n bits from the least significant bit side of the L-bit width, where L is a given natural number, and m and n are natural numbers satisfying $L = m + n$.

4. The variable length coding unit according to claim 3, wherein said variable length encoder comprises a variable length coded data cutting section for reading the n-bit code length of the variable length code from the least significant bit side of the L-bit width of said table memory, and for cutting the variable length code from the most significant bit side by a length indicated by the code length.

5. The variable length coding unit according to claim 2, wherein said table memory adds non-significant bits to an end of a variable length code with a length of less than m bits to make it m-bit data.

6. The variable length coding unit according to claim 2, wherein said processor carries out, for a less-frequently occurring event, coding of a fixed length code corresponding to the event.

7. The variable length coding unit according to claim 2, wherein

said processor carries out part of a series of variable length coding processings.

8. A variable length decoding unit comprising:

a bit stream register for storing a received bit stream;

a table memory for storing a code length of each variable length code in connection with combined data including a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients in accordance with a scanning sequence of block data consisting of a plurality of image signals;

a data reader for reading a predetermined number of bits from said bit stream register;

an address generator for generating an address of said table memory from data read from said data reader; and

a variable length decoder for reading data from the address of said table memory generated by said address generator, and for carrying out variable length decoding by cutting from the data the number of the consecutive insignificant coefficients, the value of the significant coefficient and the code length of the variable length code.

9. The variable length decoding unit according to claim 8, further comprising:

a shifter for shifting data in said bit stream register by the code length of the variable length code that is cut by said variable length decoder, to discard data by the length of the variable length code passing through the variable length decoding;

a bit stream capturing section for inserting the received

bit stream into said bit stream register without leaving any spacing between bits when said bit stream register has a space greater than a predetermined number of bits;

an image signal generator for generating the block data consisting of the plurality of image signals in response to the number of the consecutive insignificant coefficients and the value of the significant coefficient passing through the variable length decoding by said variable length decoder in accordance with the scanning sequence; and

a processor for activating and controlling at least part of said bit stream register, said data reader, said address generator, said variable length decoder, said shifter, said bit stream capturing section and said image signal generator.

10. The variable length decoding unit according to claim 9, wherein said table memory stores data that changes its bit fields associated with the number of the consecutive insignificant coefficients, with the value of the significant coefficient and with the code length of the variable length code in accordance with a coding scheme used for connecting to a party station.

11. The variable length decoding unit according to claim 9, wherein said shifter shifts data in said bit stream register toward a most significant bit side, and said bit stream capturing section inserts a bit stream into said bit stream register beginning from the most significant bit side without leaving any spacing between bits.

12. The variable length decoding unit according to claim 9, wherein said bit stream capturing section inserts the bit stream

by a predetermined number of bits.

13. The variable length decoding unit according to claim 9, wherein said bit stream register has a word width of N bits, and when inserting a bit stream whose number of significant bits is less than N into said bit stream register, said bit stream capturing section adds non-significant bits to an end of the bit stream to make the bit stream N bits wide, where N is a given natural number.

14. The variable length decoding unit according to claim 9, wherein said processor carries out decoding processing of a fixed length code.

15. The variable length decoding unit according to claim 9, wherein said processor carries out part of a series of variable length decoding processings.